OK TO ENTER: /A.S./ (10/06/2011)

IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): A method of controlling a process performed by a semiconductor processing tool, comprising:

inputting a first principles physical model including a set of computer-encoded differential equations, the first principles physical model describing at least one of a basic physical or chemical attribute of the semiconductor processing tool and including 1) a spatially resolved model of a physical geometry of the semiconductor processing tool and 2) a grid set addressing the semiconductor processing tool or a geometry of the semiconductor processing tool;

inputting process data related to an actual process being performed by the semiconductor processing tool;

setting boundary conditions for the spatially resolved model of a physical geometry of the semiconductor processing tool based on said process data related to the actua process being performed by the semiconductor processing tool;

storing in a fab-level library known simulation results obtained from simulation modules in a device manufacturing fab and distributing the known simulation results to other semiconductor processing tools in the device manufacturing fab;

solving the computer-encoded differential equations of the first principles physical model for the spatially resolved model concurrently with the actual process being performed and in a time frame shorter in time than the actual process being performed to produce a first principles simulation by: /A.S./

using code parallelization techniques on multiple simulation modules in the device manufacturing fab, and

re-using known simulation solutions as initial conditions for the first principles simulation,

wherein re-using known simulation solutions comprises searching in the fab-level library for a closest fitting solution which if used for the initial condition would reduce the number of iterations required by the simulation module;

providing from the solution of the computer-encoded differential equations solved concurrently with the actual process being performed a first principles simulation result; and

using the first principles simulation result obtained during the performance of the actual process to control the actual process performed by the semiconductor processing tool.

Claim 2 (Previously Presented): The method of Claim 1, wherein said inputting process data comprises directly inputting the data relating to the actual process being performed by the semiconductor processing tool from at least one of a physical sensor and a metrology tool physically mounted on the semiconductor processing tool.

Claim 3 (Previously Presented): The method of Claim 1, wherein said inputting process data comprises indirectly inputting the data relating to the actual process being performed by the semiconductor processing tool from at least one of a manual input device and a database.

Claim 4 (Original): The method of Claim 3, wherein said indirectly inputting comprises inputting data recorded from a process previously performed by the semiconductor processing tool.

Claim 5 (Original): The method of Claim 3, wherein said indirectly inputting comprises inputting data set by a simulation operator.

Claim 6 (Previously Presented): The method of Claim 1, wherein said inputting process data comprises inputting data relating to at least one of the physical characteristics of the semiconductor processing tool and the semiconductor tool environment.

Claim 7 (Previously Presented): The method of Claim 1, wherein said inputting process data comprises inputting data relating to at least one of a characteristic and a result of a process performed by the semiconductor processing tool.

Claim 8-9 (Cancelled).

Claim 10 (Original): The method of Claim 1, wherein said performing first principles simulation comprises performing first principles simulation concurrently with the process performed by the semiconductor processing tool.

Claim 11 (Original): The method of Claim 1, wherein said performing first principles simulation comprises performing first principles simulation independent of the process performed by the semiconductor processing tool.

Claims 12-13 (Cancelled).

Claim 14 (Original): The method of Claim 1, wherein said using the first principles simulation result comprises using the first principles simulation result to perform at least one

of detecting, and classifying a fault in the process performed by the semiconductor processing tool.

Claim 15 (Previously Presented): The method of Claim 1, further comprising using a network of interconnected resources inside a semiconductor device manufacturing facility to perform the first principles simulation recited in Claim 1.

Claim 16 (Original): The method of Claim 15, further comprising using code parallelization among interconnected computational resources to share the computational load of the first principles simulation.

Claim 17 (Original): The method of Claim 15, further comprising sharing simulation information among interconnected resources to control the process performed by the semiconductor processing tool.

Claim 18 (Original): The method of Claim 17, wherein said sharing simulation information comprises distributing simulation results among the interconnected resources to reduce redundant execution of substantially similar first principles simulations by different resources.

Claim 19 (Original): The method of Claim 17, wherein said sharing simulation information comprises distributing model changes among the interconnected resources to reduce redundant refinements of first principles simulations by different resources.

Claim 20 (Previously Presented): The method of Claim 1, further comprising using remote resources via a wide area network to control the semiconductor process performed by the semiconductor processing tool.

Claim 21 (Previously Presented): The method of Claim 20, wherein said using remote resources comprises using at least one of remote computational and storage resources via a wide area network to facilitate the semiconductor process performed by the semiconductor processing tool.

Claim 22 (Original): The method of Claim 1, wherein said performing first principles simulation utilizes at least one of an ANSYS computer code, a FLUENT computer code, a CFRDC-ACE computer code, and a direct simulation Monte Carlo computer code.

Claim 23 (Currently Amended): The method of Claim 1, wherein said performing first principles simulation comprises: /A.S./

calculating a solution to the first principles simulation by applying said ~~close~~closest-fitting solution to thereby set the initial conditions for cells in the first principles simulation.

Claim 24 (Currently Amended): The method of Claim 23, wherein said calculating comprises:

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selecting said ~~close~~closest-fitting solution from a library of solutions.

Claim 25 (Original): The method of Claim 24, wherein said selecting comprises:

selecting a solution from the library of solutions that has proven convergence on the semiconductor processing tool.

Claim 26 (Currently Amended): The method of Claim 23, wherein said selecting comprises: /A.S./

selecting said ~~close~~closest-fitting solution from a library of solutions existing on a network of computers connected to said semiconductor processing tool.

Claim 27 (Original): The method of Claim 1, wherein said performing first principles simulation comprises:

calculating a solution to the first principles simulation by choosing a coarse grid for solution to the first principles simulation.

Claim 28 (Previously Presented): The method of Claim 27, wherein said calculating a solution further comprises:

utilizing the solution of the coarse grid to set the initial conditions for cells in a subsequent first principles simulation using a fine grid.

Claim 29 (Original): The method of Claim 1, wherein said using the first principles simulation result to control the process comprises:

performing a principle components analysis to determine a relationship between spatial components of said first principles simulation result for the semiconductor processing tool and a set of at least one control variable, said relationship utilized to determine a correction to said set of at least one control variable in order to affect a reduction in the magnitude of said spatial components.

Claim 30 (Original): The method of Claim 1, wherein said using the first principles simulation result to control comprises:

controlling at least one of a material processing system, an etch system, a photoresist spin coating system, a lithography system, a dielectric coating system , a deposition system , a rapid thermal processing system for thermal annealing, and a batch diffusion furnace.

Claim 31 (Original): The method of Claim 30, wherein said using the first principles simulation result to control comprises:

controlling at least one of a chemical vapor deposition system and a physical vapor deposition system.

Claim 32 (Original): The method of Claim 1, further comprising:

inputting as tool data at least one of etch rate, deposition rate, etch selectivity, an etch critical dimension, an etch feature anisotropy , a film property, a plasma density, an ion energy, a concentration of a chemical specie, a photoresist mask film thickness, a photoresist pattern dimension.

Claim 33 (Original): The method of Claim 1, wherein said inputting data comprises:

inputting physical geometric parameters of at least one of a material processing system, an etch system, a photoresist spin coating system, a lithography system, a dielectric coating system, a deposition system , a rapid thermal processing system for thermal annealing, and a batch diffusion furnace.

Claim 34 (Original): The method of Claim 1, wherein said using the first principles simulation result to control comprises:

controlling the semiconductor processing tool by using model output to adjust said process performed by the semiconductor processing tool.

Claim 35 (Original): The method of Claim 34, wherein said controlling comprises:

utilizing at least one of nonlinear optimization and multivariate analysis to derive a control model for process control.

Claim 36 (Original): The method of Claim 1, further comprising:

exchanging information between a plurality of computing/storage devices including at least one of model solver parameters, solution status to the first principles simulation, model solutions to the first principles simulation, and solution convergence history for said model solutions.

Claim 37 (Original): The method of Claim 1, further comprising:

inspecting process results; and

providing input to the first principles simulation for calibration purposes.

Claim 38 (Currently Amended): A system comprising:

a semiconductor processing tool configured to perform a process;

a fab-level library storing known simulation results obtained from simulation modules in a device manufacturing fab;

a fab-level process controller distributing the known simulation results to other semiconductor processing tools in the device manufacturing fab;

a first principles simulation processor configured to input a first principles physical model including a set of computer-encoded differential equations describing at least one of a

basic physical or chemical attribute the semiconductor processing tool and including 1) a spatially resolved model of a physical geometry of the semiconductor processing tool and 2) a grid set addressing the semiconductor processing tool or a geometry of the semiconductor processing tool;

an input device configured to input process data related to an actual process being performed by the semiconductor processing tool; and

said first principles simulation processor further configured to:

set boundary conditions for the spatially resolved model of a physical geometry of the semiconductor processing tool based on said process data related to the actual process being performed by the semiconductor processing tool,

solve the computer-encoded differential equations of the first principles physical model for the spatially resolved model concurrently with the actual process being performed and in a time frame shorter in time than the actual process being performed to produce a first principles simulation by: /A.S./

using code parallelization techniques on multiple simulation modules in the device manufacturing fab, and

re-using known simulation solutions as initial conditions for the first principles simulation,

wherein re-using known simulation solutions comprises searching in the fab-level library for a closest fitting solution which if used for the initial condition would reduce the number of iterations required by the simulation module,

provide from the solution of the computer-encoded differential equations solved concurrently with the actual process being performed a first principles simulation result,

wherein said first principles simulation result obtained during the performance of the actual process is used to control the actual process performed by the semiconductor processing tool.

Claim 39 (Original): The system of Claim 38, wherein said input device comprises at least one of a physical sensor and a metrology tool physically mounted on the semiconductor processing tool.

Claim 40 (Original): The system of Claim 38, wherein said input device comprises at least one of a manual input device and a database.

Claim 41 (Original): The system of Claim 40, wherein said input device is configured to input data recorded from a process previously performed by the semiconductor processing tool.

Claim 42 (Original): The system of Claim 40, wherein said input device is configured to input data set by a simulation operator.

Claim 43 (Original): The system of Claim 38, wherein said input device is configured to input data relating to at least one of the physical characteristics of the semiconductor processing tool and the semiconductor tool environment.

Claim 44 (Original): The system of Claim 38, wherein said input device is configured to input data relating to at least one of a characteristic and a result of a process performed by the semiconductor processing tool.

Claims 45-46 (Cancelled).

Claim 47 (Original): The system of Claim 38, wherein said processor is configured to perform said first principles simulation concurrently with the process performed by the semiconductor processing tool.

Claim 48 (Previously Presented): The system of Claim 38, wherein said processor is configured further to perform said first principles simulation not concurrently with the process performed by the semiconductor processing tool.

Claims 49-50 (Cancelled).

Claim 51 (Original): The system of Claim 38, wherein said processor is configured to use the first principles simulation result to perform at least one of detecting, and classifying a fault in the process performed by the semiconductor processing tool.

Claim 52 (Previously Presented): The system of Claim 38, further comprising a network of interconnected resources inside a semiconductor device manufacturing facility and connected to said processor and configured to assist said processor in performing at least one of the inputting a first principles simulation model and performing a first principles simulation.

Claim 53 (Original): The system of Claim 52, wherein said network of interconnected resources is configured to use code parallelization with said processor to share the computational load of the first principles simulation.

Claim 54 (Original): The system of Claim 52, wherein said network of interconnected resources is configured to share simulation information with said processor to facilitate said process performed by the semiconductor processing tool.

Claim 55 (Original): The system of Claim 54, wherein said network of interconnected resources is configured to distribute simulation results to said processor to reduce redundant execution of substantially similar first principles simulations.

Claim 56 (Original): The system of Claim 54, wherein said network of interconnected resources is configured to distribute model changes to said processor to reduce redundant refinements of first principles simulations.

Claim 57 (Previously Presented): The system of Claim 38, further comprising remote resources connected to said processor via a wide area network and configured to facilitate the semiconductor process performed by the semiconductor processing tool.

Claim 58 (Original): The system of Claim 57, wherein said remote resources comprise at least one of a computational and a storage resource.

Claim 59 (Original): The system of Claim 38, wherein said processor is configured to perform first principles simulation utilizes at least one of an ANSYS computer code, a

FLUENT computer code, a CFRDC-ACE computer code, and a direct simulation Monte Carlo computer code.

Claim 60 (Currently Amended): The system of Claim 38, wherein said processor is configured to perform first principles simulation at least by calculating a solution to the first principles simulation by applying said ~~eloseclosest~~-fitting solution to thereby set the initial conditions for cells in the first principles simulation. /A.S./

Claim 61 (Currently Amended): The system of Claim 60, wherein said processor is configured to perform said calculating by at least selecting said ~~eloseclosest~~ -fitting solution from a library of solutions. /A.S./

Claim 62 (Original): The system of Claim 61, wherein said processor is configured to perform said selecting by at least selecting a solution from the library of solutions that has proven convergence on the semiconductor processing tool.

Claim 63 (Currently Amended): The system of Claim 60, wherein said processor is configured to perform said selecting by at least selecting said ~~eloseclosest~~-fitting solution from a library of solutions existing on a network of computers connected to said semiconductor processing tool. /A.S./

Claim 64 (Original): The system of Claim 38, wherein said processor is configured to perform first principles simulation by at least calculating a solution to the first principles simulation by choosing a coarse grid for solution to the first principles simulation.

Claim 65 (Previously Presented): The system of Claim 64, wherein said processor is configured to perform calculating a solution by at least utilizing the solution of the coarse grid to set the initial conditions for cells in a subsequent first principles simulation using a fine grid.

Claim 66 (Original): The system of Claim 38, wherein said processor is configured to use the first principles simulation result to control the process by at least performir g a principle components analysis to determine a relationship between spatial components of said first principles simulation result for the semiconductor processing tool and a set of at least one control variable, said relationship utilized to determine a correction to said set of at least one control variable in order to affect a reduction in the magnitude of said spatial components.

Claim 67 (Original): The system of Claim 38, wherein said processor is configured to use the first principles simulation result to control the process by at least controlling at least one of a material processing system, an etch system, a photoresist spin coating system, a lithography system, a dielectric coating system, a deposition system , a rapid thermal processing system for thermal annealing, and a batch diffusion furnace.

Claim 68 (Original): The system of Claim 67, wherein said processor is configured to use the first principles simulation result to control the process by controlling at least one of a chemical vapor deposition system and a physical vapor deposition system.

Claim 69 (Original): The system of Claim 38 wherein said input device is configured to input at least one of etch rate, deposition rate, etch selectivity, an etch critical dimension,

an etch feature anisotropy, a film property, a plasma density, an ion energy, a concentration of a chemical specie, a photoresist mask film thickness, a photoresist pattern dimension.

Claim 70 (Original): The system of Claim 38, wherein said input device is configured to input physical geometric parameters of at least one of a material processing system, an etch system, a photoresist spin coating system, a lithography system, a dielectric coating system, a deposition system , a rapid thermal processing system for thermal annealing, and a batch diffusion furnace.

Claim 71 (Original): The system of Claim 38, wherein said processor is configured to use the first principles simulation result to control the process by at least controlling the semiconductor processing tool by using model output to adjust said process performed by the semiconductor processing tool.

Claim 72 (Original): The system of Claim 71, wherein said processor configured to perform said controlling by utilizing at least one of nonlinear optimization and multivariate analysis to derive a control model for process control.

Claim 73 (Original): The system of Claim 38, wherein said processor is further configured to exchange information between a plurality of computing/storage devices including at least one of model solver parameters, solution status to the first principles simulation, model solutions to the first principles simulation, and solution convergence history for said model solutions.

Claim 74 (Original): The system of Claim 38, wherein said processor is further configured to:

inspect process results; and

provide input to the first principles simulation for calibration purposes.

Claims 75 - 77 (Cancelled).

Claim 78 (Currently Amended): At least one of non-volatile media and volatile media containing program instructions for execution on a processor, which when executed by the a /A.S./ computer system, cause the processor to perform the steps of:

inputting a first principles physical model including a set of computer-encoded differential equations, the first principles physical model describing at least one of a basic physical or chemical attribute of the semiconductor processing tool and including 1) a spatially resolved model of a physical geometry of the semiconductor processing tool and 2) a grid set addressing the semiconductor processing tool or a geometry of the semiconductor processing tool;

inputting process data related to an actual process being performed by the semiconductor processing tool;

setting boundary conditions for the spatially resolved model of a physical geometry of the semiconductor processing tool based on said process data related to the actual process being performed by the semiconductor processing tool;

storing in a fab-level library known simulation results obtained from simulation modules in a device manufacturing fab and distributing the known simulation results to other semiconductor processing tools in the device manufacturing fab;

solving the computer-encoded differential equations of the first principles physical model for the spatially resolved model concurrently with the actual process being performed

and in a time frame shorter in time than the actual process being performed to produce a first principles simulation by: /A.S./

using code parallelization techniques on multiple simulation modules in the device manufacturing fab, and

re-using known simulation solutions as initial conditions for the first principles simulation,

wherein re-using known simulation solutions comprises searching in the fab-level library for a closest fitting solution which if used for the initial condition would reduce the number of iterations required by the simulation module;

providing from the solution of the computer-encoded differential equations solved concurrently with the actual process being performed a first principles simulation result; and

using the first principles simulation result obtained during the performance of the actual process to control the actual process performed by the semiconductor processing tool.

Claims 79-81 (Cancelled).